Name of Programme: Competitive Research Programme
Proposal ID: CRP20-2017-0006
Project Title: CogniVision – Energy-autonomous always-on cognitive and attentive cameras for distributed real-time vision with milliwatt power consumption
Name of Lead PI: Assoc Prof. Massimo Alioto
Host Institution: National University of Singapore
Faculty & Department: Faculty of Engineering, Department of Electrical and Computer Engineering

Summary of Budget Request	Amount
Total Direct Cost	$5,908,750.00
Research Scholarship (Items Not Eligible for Indirect Cost)	$432,000.00
Total Qualifying Approved Direct Cost ('Total Direct Cost' less 'Items Not Eligible	$5,476,750.00
Indirect Cost (20% of Total Qualifying Approved Direct Cost)	$1,095,350.00
Total Project Cost (Total Direct Cost + Indirect Cost)	$7,004,100.00

EXPENDITURE ON MANPOWER (EOM)

Item No.	Category	Number of Pax	Annual salary package	[redacted]	Year 1 Please input the amount as shown under Year 1, and leave Year 2, 3, 4, 5 blank	Total Cost	Description Please include details for each line item on: 1. Total man-months for the project duration. 2. Role of this manpower. 3. How this manpower ties with the deliverables and milestones.
EOM-001	Research Fellow	1	$85,000.00		$424,800.00	$424,800.00	Research Fellow: 1RF (yr 1-5) contributing to system-level aspects and integration tasks {1.1-1.6}
EOM-002	Research Fellow	1	$85,000.00		$424,800.00	$424,800.00	Research Fellow: 1RF (yr 1-5) contributing to system simulation and design tasks {1.1, 1.5, 1.6}
EOM-003	Research Fellow	1	$85,000.00		$424,800.00	$424,800.00	Research Fellow: 1RF (yr 1-5) works on research on imager/transceiver circuit/architecture tasks {2.1-2.5}
EOM-004	Research Engineer	1	$64,000.00		$319,800.00	$319,800.00	Research Engineer: 1RA (yr 1-5) contributing to imager tasks {2.1, 2.2, 2.3, 2.4, 2.5}
EOM-005	Research Engineer	1	$64,000.00		$319,800.00	$319,800.00	Research Engineer: 1RA (yr 1-5) contributing to transceiver tasks {2.1, 2.2, 2.3, 2.4, 2.5}
EOM-006	Research Fellow	1	$85,000.00		$254,880.00	$254,880.00	Research Fellow: 1RF (yr 1-3) research on deep learning models and saliency tasks {3.1-3.3}
EOM-007	Research Fellow	1	$85,000.00		$254,880.00	$254,880.00	Research Fellow: 1RF (yr 3-5) research on deep learning training, benchmarking tasks {3.3, 3.4}
EOM-008	Research Fellow	1	$85,000.00		$191,880.00	$191,880.00	Research Fellow: 1RF (yr 1-3) development of deep learning models and saliency tasks {3.1-3.3}
EOM-009	Research Engineer	1	$64,000.00		$191,880.00	$191,880.00	Research Engineer: 1RA (yr 3-5) development of deep learning training, benchmarking tasks {3.3, 3.4}
EOM-010	Research Fellow	1	$85,000.00		$424,800.00	$424,800.00	Research Fellow: 1RF (yr 1-5) contributing on architectural and system-level activity skipping/EQ tasks {4.1-4.5}
EOM-011	Research Engineer	1	$64,000.00		$319,800.00	$319,800.00	Research Engineer: 1RA (yr 1-5) circuit-level optimization, verification of activity skipping/EQ tasks {4.1-4.5}
EOM-012	Research Engineer	1	$64,000.00		$256,000.00	$256,000.00	Research Engineer: 1RA (yr 1-4) gate-level optimization, testing of activity skipping/EQ tasks {4.1-4.5} EOM-12 (Research Engineer) contributes to the tasks 4.1-4.5, which aim to investigate and demonstrate the enabling digital circuit technologies for cognitive cameras. The investigation and the demonstration of such techniques are essential to reach the power consumption goals detailed in the proposal (see, e.g., the project title), via very energy-efficient on-chip computation. From a milestone viewpoint, EOM-12 is indispensable to achieve M4.1, M4.2, M4.3, M4.4, as they all involve the exploration and the design of the digital sub-system at the gate/micro-architectural level (this will be executed in parallel with the circuit and architectural work by EOM-010 and EOM-011, to cover the entire range from circuit to micro-architecture and architecture). Reviewing the schedule and the roles of the manpower, the above considerations apply to EOM-12 for the first four years, whereas the fifth year can be somewhat managed by EOM-10 and EOM-11 (once all final version of the RTL designs are made available by EOM-12). In other words, it would be sufficient to support EOM-12 for four years, instead of the overall period of five years.
				Total Cost for EOM		$3,808,120.00	

JUSTIFICATIONS FOR EOM CATEGORY

Please provide reasons to justify and support the need to recruit for each of the manpower line item (limit to 4000 characters).

EOM-001 1RF (yr 1-5) contributing to system-level aspects and integration tasks {1.1-1.6}
EOM-002 1RF (yr 1-5) contributing to system simulation and design tasks {1.1, 1.5, 1.6}
EOM-003 1RF (yr 1-5) works on research on imager/transceiver circuit/architecture tasks {2.1-2.5}
EOM-004 1RA (yr 1-5) contributing to imager tasks {2.1, 2.2, 2.3, 2.4, 2.5}
EOM-005 1RA (yr 1-5) contributing to transceiver tasks {2.1, 2.2, 2.3, 2.4, 2.5}
EOM-006 1RF (yr 1-3) research on deep learning models and saliency tasks {3.1-3.3}
EOM-007 1RF (yr 3-5) research on deep learning training, benchmarking tasks {3.3, 3.4}
EOM-008 1RF (yr 1-3) development of deep learning models and saliency tasks {3.1-3.3}
EOM-009 1RA (yr 3-5) development of deep learning training, benchmarking tasks {3.3, 3.4}
EOM-010 1RF (yr 1-5) contributing on architectural and system-level activity skipping/EQ tasks {4.1-4.5}
EOM-011 1RA (yr 1-5) circuit-level optimization, verification of activity skipping/EQ tasks {4.1-4.5}
EOM-012 1RA (yr 1-4) gate-level optimization, testing of activity skipping/EQ tasks {4.1-4.5}

EQUIPMENT (EQP)

Item No.	Category	[redacted]	Total Units	Cost Per Unit	Total Cost	Description Please include details for each line item on: 1. Name of Equipment (if "Others (Please specify) is selected). 2. Description of the item to be purchased. 3. Whether this equipment exists in the Host / Participating Institutions. 4. How this item will tie with the deliverables and milestones.
EQP-001	Others (Please specify)		6	$10,000.00	$60,000.00	GPU workstations/servers: Deep learning network training, system simulations. The high-performance GPU workstations/servers are necessary to perform both training and inference on neural networks, as required by Sub-projects 3 and 4. These items have a very high-performance requirement (in terms of CPUs and GPUs), to execute design, training and inference in a reasonable time. In contrast, a general-purpose desktop computer would take weeks to train one neural network instance (e.g., AlexNet), hence design exploration requires an order of magnitude speed-up, to meet the timeline indicated in the Gantt chart. Being very different, these computers do not belong to the category of general-purpose IT.
EQP-002	Others (Please specify)		1	$209,130.00	$209,130.00	Measurement equipment for testchip characterization: comprising National Instruments integrated equipment for timing characterization, testing, power characterization. The quotation for a tentative configuration is now provided as EQP-002.pdf (it can also be downloaded at www.ni.com/advisor/retrieve/ - please, insert configuration PX5796458 to visualize it). Being delivered by a sole distributor (National Instruments), only one quotation is available for the integrated testing equipment. The cost will be within the budget indicated in this spreadsheet, once educational discount is applied. Consider that the configuration is only tentative at this stage, as careful choice of measurement cards will have to be made based on the preliminary research exploration (tasks 1.1, 2.1, 2.2), based on which the testbed will be defined in detail to fit and fully support the targeted chip architecture. Among the other possible changes, addition of a load board and cards for RF testing will be considered during the definition of the simulation and testing framework in the execution of the above tasks. The equipment is necessary to support the following objectives: - testchip characterization of imager, digital and radio-frequency sub-systems - testing and characterization of system on chip comprising the various sub-systems - testing and characterization of ultra-low energy architectures with energy-quality scalability. The equipment is also necessary for the following deliverables (see Annex C1): - Integrated circuit performing feature extraction at 50 µW power (or lower) at VGA resolution, 5fps frame rate - saliency assessment engine with 80 µW power at VGA resolution, 5pfs frame rate - mager with 100 µW power (VGA, 30 fps) at activity rate of average NeoVision2 benchmark - Integrated circuit performing image sensing and scene analysis with average power consumption in the mW range, including neural acceleration with maximum accuracy no lower than the best-in-class detection/classification algorithms minus 5-10% (indoor, 500-lux lighting, max. 20 people).
EQP-003	Others (Please specify)		1	$5,000.00	$5,000.00	Racks and network switch for servers: The racks and network switch for servers is necessary for the installation of the latter ones, and will hence support all tasks that servers will be used for: - simulations (tasks 1.1, 1.2, 2.1, 2.2, 4.1, 4.2) - design (tasks 1.3, 2.3, 4.3, 4.4).
EQP-004	Others (Please specify)		5	$15,000.00	$75,000.00	Servers for chip design: necessary for circuit simulation/design, 5 server blades are needed for 5 simultaneous designers. The servers will support all simulation/design-related tasks: - simulations (tasks 1.1, 1.2, 2.1, 2.2, 4.1, 4.2) - design (tasks 1.3, 2.3, 4.3, 4.4).
EQP-005	Others (Please specify)		4	$3,000.00	$12,000.00	Workstations: The servers will support all simulation/design-related tasks, for local processing and access to servers: - simulations (tasks 1.1, 1.2, 2.1, 2.2, 4.1, 4.2) - design (tasks 1.3, 2.3, 4.3, 4.4). Monitors need to be very large size (e.g., 43") to allow layout of complex circuits and the overall system on chip. These workstations do not belong to the category of general-purpose IT, in view of their high-performance/fast-storage, very large screen and multi-screen requirements, as necessary to run compute-intenstive chip design CAD tools for complex systems on chip, and to seamlessly access servers.
				Total Cost for EQP	$361,130.00	

JUSTIFICATIONS FOR EQUIPMENT CATEGORY

Please indicate if each of the equipment is currently available in the institution. If yes, please justify the need to purchase similar equipment.

Please provide reasons to justify and support the need to purchase each of the equipment. (limit to 4000 characters)

o GPU workstations/servers: deep learning network training, system simulations
o Measurement equipment for testchip characterization comprising National Instruments integrated equipment for timing characterization, testing, power characterization
o Racks and network switch for servers
o Servers for chip design, necessary for circuit simulation/design
o Workstations with monitors for research staff

OTHER OPERATING EXPENSES (OOE)

Item No.	Category	[redacted]	Total Cost	Description Please include details for each line item on: 1. Name of OOE item (if "Others (Please specify) is selected). 2. Description of the item to be purchased. 3. How this item will tie with the deliverables and milestones.
OOE-001	Others (Please specify)		$7,000.00	Computer accessories (external HD for backup, NAS, other peripherals for productivity, storage, etc.) are needed for ordinary needs. The accessories in this item cannot be supported by the School/Faculty, as they are not part of standard computer configurations. In detail, these accessories are needed for example to backup and organize large quantities of shared data (e.g., vision benchmarks, neural networks), including (and not limited to) Network Attached Systems, server backup systems, and UPS to preserve data integrity in the presence of computer/storage faults (which are likely to happen in the 5-year lifespan of the project).
OOE-002	Others (Please specify)		$40,500.00	Printed Circuit Board fabrication, chip packaging, miscellaneous electronics Printed Circuit Board fabrication/assembly is necessary to test silicon chips, as they are designed to implement the peripheral circuitry and the connectors at the scale of testing equipment, as routine step required before chip characterization. Chip packaging/3D stacking/system-in-package integration is routinely needed to test silicon chips, to assemble them into components that can be used in Printed Circuit Boards for testing through commercial testing equipment. Miscellaneous electronics is routinely needed to test silicon chips, and includes components (electrical and not) required for the chip testing, such as capacitors, resistors, voltage regulators, transistors, microcontrollers, legs for PCBs, and equivalent. All above items are indispensable for chip testing, and are part of the usual testing cycle of chips.
OOE-003	Others (Please specify)		$10,000.00	Publication fees
OOE-004	Others (Please specify)		$1,100,000.00	Silicon manufacturing for chip prototyping: testchip fabrication in CMOS technology (targeted: 28 nm). Two rounds of prototyping are needed for 1) imager and 2) sensemaking. Their merge into the final chip demo takes 1.5X the area of each. Silicon manufacturing is necessary to build the silicon chips designed in our labs, as routine activity related to silicon demonstration (an essential part of the project). As mentioned in the final proposal, the choice of the silicon foundry and the specific technology tightly depends on aspects related to system performance, availability and alignment of manufacturing runs with the project schedule, as well as adoption of a common technology across the groups belonging to the team. The item supports the following objectives (see Annex C1): - chip demonstration of low-level scene analysis building blocks - system on chip demonstration of a complete cognitive camera. The item supports the following deliverables (see Annex C1): - Integrated circuit performing feature extraction at 50 µW power (or lower) at VGA resolution, 5fps frame rate - saliency assessment engine with 80 µW power at VGA resolution, 5pfs frame rate - imager with 100 µW power (VGA, 30 fps) at activity rate of average NeoVision2 benchmark - Integrated circuit performing image sensing and scene analysis with average power consumption in the mW range, including neural acceleration with maximum accuracy no lower than the best-in-class detection/classification algorithms minus 5-10% (indoor, 500-lux lighting, max. 20 people).
OOE-005	Others (Please specify)		$15,000.00	Visiting Professor (Collaborator: Prof. Sylvester) Prof. Sylvester will contribute to the research focused on energy-efficient circuits, and hence to the following objectives/deliverables (see Annex C1, Prof. Sylvester's CV at https://web.eecs.umich.edu/~dennis/cv_full_Dennis_8-2014.pdf): - imager with 100 µW power (VGA, 30 fps) at activity rate of average NeoVision2 benchmark - Integrated circuit performing feature extraction at 50 µW power (or lower) at VGA resolution, 5fps frame rate - saliency assessment engine with 80 µW power at VGA resolution, 5pfs frame rate. In detail, Prof. Sylvester will contribute to the tasks 4.1, 4.2, 4.3, 4.4.
OOE-006	Others (Please specify)		$15,000.00	Visiting Professor (Collaborator: Prof. Benini) Prof. Benini will contribute to the research focused on energy-efficient architectures, and hence to the following objectives/deliverables (see Annex C1, Prof. Luca Benini's CV at https://www.ethz.ch/content/dam/ethz/special-interest/itet/department/Department/Professors/Factsheet_Final/Benini_Factsheet_Final.pdf): - system on chip demonstration of a complete cognitive camera - Integrated circuit performing image sensing and scene analysis with average power consumption in the mW range, including neural acceleration with maximum accuracy no lower than the best-in-class detection/classification algorithms minus 5-10% (indoor, 500-lux lighting, max. 20 people). In detail, Prof. Benini will contribute to the tasks 1.2, 1.3, 3.1.
		Total Cost for OOE	$1,187,500.00	

JUSTIFICATIONS FOR OOE CATEGORY

Please provide reasons to justify and support the need to purchase each of the OOE item. (limit to 4000 characters)

o Computer peripherals/accessories: computer accessories (external HD for backup, NAS, other peripherals for productivity, storage, etc.) are needed for ordinary needs
o Printed Circuit Board fabrication, chip packaging, miscellaneous electronics
o Publication fees
o Silicon manufacturing for chip prototyping: testchip fabrication in CMOS technology (targeted: 28 nm). Two rounds of prototyping are needed for imager/transceiver and sensemaking (S$ 200K/tapeout in 28mm2). Merge into final chip takes 1.5X the area of each
o Visiting professors (collaborators)

OVERSEAS TRAVEL (OT)

Item No.	[redacted]	Total Cost	Description Please include details for each line item on: 1. Description of the item. 2. How this item will tie with the deliverables and milestones
OT-001		$120,000.00	Overseas Conferences and Working Visits: Trips for the three PIs (for conference attendance, technical meetings, talks strictly relevant to the project) Attendance of overseas conferences that are strictly related to the project's area of research and specific objectives. This simultaneously serves the purposes of disseminating the scientific results produced, continuing to be current with the advances in the state of the art in the project's field, attending world-class seminars/courses to acquire otherwise unavailable knowledge, enhancing visibility of the project (e.g., giving invited talks and keynotes). Example of conferences that are relevant to the project's field and objectives are IEEE ISSCC, IEEE VLSI Symposium, IEEE ASSCC, IEEE ISCAS, IEEE RFIC, NIPS, ICML, conferences/workshops organized by industry (e.g., Embedded Vision Alliance yearly summit), and other related conferences. Working visits to academic and industrial groups are crucial to gain publically unavailable insights on recent advances (e.g., unpublished) and the technology ecosystem in the specific field (e.g., to steer reasearch in directions that maximize the impact of the project). Examples of working visits include semiconductor companies (e.g., TSMC, Intel, ARM...), universities (e.g., Stanford, Berkeley, UIUC, MIT), and system integrators (e.g., Panasonic), and other equivalent major players in the field.
	Total Cost for OT	$120,000.00	

JUSTIFICATIONS FOR OT CATEGORY

Please provide reasons to justify and support the need for each of the OT item. (limit to 4000 characters)

Trips for the three Pis (for conference attendance, technical meetings, talks strictly relevant to the project). A tentative breakdown (which will be highly influenced by the project progress and timing in individual tasks and related interaction) is as follows: 20 conferences, 4 talks, 5 technical meetings (including collaborators)

RESEARCH SCHOLARSHIP (RS) ***(Not Eligible for Indirect Cost)***

Item No.	Category	Number of Pax	Annual Cost per pax	Average Monthly Cost per pax	Total Man-months	Total Cost	Description Please include details for each line item on: 1. Total man-months for the project duration. 2. Role of this manpower. 3. How this manpower ties with the deliverables and milestones.
RS-001	PhD Student	1	$54,000.00	$4,500.00	48	$216,000.00	PhD Student : 1RS (yr 1-4) on energy-autonomous integrated system modelling, design and optimization for real-time video processing tasks {1.2, 1.3, 1.4, 1.5, 1.6}
RS-002	PhD Student	1	$54,000.00	$4,500.00	48	$216,000.00	PhD Student : 1RS (yr 1-4) on energy-aware integrated circuit design for machine learning and real-time on-chip analytics tasks {1.2, 1.3, 1.4, 1.5, 1.6}
					Total Cost for RS	$432,000.00	

JUSTIFICATIONS FOR RS CATEGORY

Please provide reasons to justify and support the need to recruit for each of the manpower line item. (limit to 4000 characters)

2RS (yr 1-4) on energy-autonomous integrated system modelling, design and optimization for real-time video processing tasks {1.2, 1.3, 1.4, 1.5, 1.6}

Submission No.:
Final Submission

Date of Submission:
24-Dec-18