CURRICULUM VITAE

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CURRENT POSITION: Associate Professor at ECE, Faculty of Engineering, National University of Singapore (since July 1, 2013), full time (100% time spent in Singapore every year)

EMPLOYMENT HISTORY

- Visiting Scientist, Circuit Research Lab - Intel Labs, Hillsboro, OR (01/2013 – 03/2013)
- Visiting Professor, EECS - University of Michigan – Ann Arbor (07/2011 – 12/2012)
- Visiting Professor, Berkeley Wireless Research Center, University of California - Berkeley (05/2009 – 07/2011)
- Associate Professor, Dept. of Information Engineering, University of Siena - Italy (promoted in 2005, at age 32 – youngest Italian Associate Professor in EE)
- Visiting Professor, Laboratory of Integrated Systems, EPF Lausanne - Switzerland (07/2007 – 08/2007)
- Assistant Professor, Dept. of Information Engineering, University of Siena - Italy (10/2002 - 9/2006)

ACADEMIC QUALIFICATIONS

- Masters degree in Electronic Engineering (specialization in Microelectronics), University of Catania (Italy), 1997
- Ph.D. degree in Electrical Engineering, University of Catania (Italy), 2001

RESEARCH INTERESTS:

- energy-centric VLSI design
- energy-autonomous systems for distributed sensing/ubiquitous computing with perpetual operation
- near-threshold integrated circuits and systems for mobile applications and IoT
- hardware-level security
- algorithm-circuit co-design for low-energy processing
- post-CMOS technologies for green computing

LIST OF 5 MOST SIGNIFICANT PUBLICATIONS IN THE PAST 3 YEARS RELEVANT TO THE PROPOSAL (5, out of total 240+, including 3 Springer books)

- S. Jain, L. Longyang, M. Alioto, “Dynamically Adaptable Pipeline for Energy-Efficient Microarchitectures under Wide Voltage Scaling,” IEEE Journal of Solid-State Circuits, vol. 53, no. 2, pp. 632-641, Feb. 2018
- Y. Zhang, M. Khayatzadeh, K. Yang, M. Saligane, N. Pinckney, M Alioto, D. Blaauw, D. Sylvester, “iRazor: Current-Based Error Detection and Correction Scheme for PVT variation

in 40-nm ARM Cortex-R4 Processor," IEEE Journal of Solid-State Circuits, vol. 53, no. 2, pp. 619-631, Feb. 2018

- L. Lin, S. Jain, M. Alioto, "Reconfigurable Clock Networks for Random Skew Mitigation from Sub-Threshold to Nominal Voltage," in IEEE ISSCC Dig. Tech. Papers, Feb. 2017, pp. 440-441
- A. Alvarez, G. Ponnusamy, M. Alioto, "EQSCALE: Energy-Quality Scalable Feature Extraction Engine for Sub-mW Real-time Video Processing with 0.55 mm2 Area in 40nm CMOS," in Proc. of ASSCC 2017, pp. 241-244 , Seoul (Korea), Nov. 2017
- W. Zhao, Y. Ha, M. Alioto, "Novel Self-Body-Biasing and Statistical Design for Near-Threshold Circuits With Ultra Energy-Efficient AES as Case Study," IEEE Trans. on VLSI Systems, vol. 23, no. 8, pp. 1390-1401, Aug. 2015.

PATENTS

Currently 2 patents filed in the US, 3 invention disclosures in Singapore.

PROFESSIONAL AWARDS

- IEEE Fellow for contributions on "energy-efficient VLSI circuits"
- Associate Editor in Chief of IEEE Trans. on VLSI Systems (2013-2018)
- Deputy Editor in Chief of IEEE Journal on Emerging and Selected Topics in Circuits and Systems (2018 onwards)
- Technical Program Committee member of the ISSCC conference (Digital Circuits subcommittee)
- Technical Program Chair of various IEEE conferences (SOCC, ICECS, PRIME, etc.)
- several keynotes at IEEE conferences, 50+ talks in last 5 years in top universities/companies
- best paper award at ACM/IEEE SBCCI 2014 conference (Aracaju, Brazil – Sept. 2014)
- Distinguished Lecturer of the IEEE Circuits and Systems Society for years 2009 and 2010
- ISCAS2010 Best Tutorial award (related invited paper opens IEEE TCAS-I 2012 editorial year)

SUMMARY OF MOST RELEVANT RESEARCH OUTCOMES FROM ALL PREVIOUS GRANTS

In the last four years, he has acquired 6+M$ of funding in Singapore. Through grants in Singapore, his research has led to a range of innovative scientific results and impactful technologies, such as innovative approaches to reconfigure digital microarchitectures to adapt to a wide range of energy-performance targets, from minimum-energy operation to maximum speed (funded by Intel). In the field of hardware-level security, Prof. Alioto's group leads also the state of the art of Physically Unclonable Functions, and AES cryptographic core for IoT with lowest energy ever reported (funded by MINDEF and MOE). Prof. Alioto is also a pioneer in the field of energy-quality scalable integrated circuits and systems, from on-chip memories to computer vision, Analog-to-Digital Converters and miniaturized systems for real-time audio processing (funded by MOE). Prof. Alioto's group is also demonstrating the first millimeter-sized and nearly-perpetual CO2 sensor for air quality monitoring in green buildings (funded by the SinBerBEST CREATE center).

At the end of 2017, his group has demonstrated the first feature extractor for IoT vision with sub-mW power (20X lower than state of the art). In early 2018, Prof. Alioto's group has demonstrated the first battery-indifferent integrated system that can continue to operate correctly even when the battery runs out of energy, thanks to a tiny on-chip solar cell and a microcontroller consuming less than 1 nW (lowest ever reported to date).