***SEMINAR ANNOUNCEMENT***

**DEPARTMENT OF ELECTRICAL AND COMPUTER**

***Area: Integrated Circuits and Embedded Systems***
***Host: Prof. Massimo Alioto***

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| **TOPIC** | **Device-Circuit Co-design of Multi-Gate FETs in Scaled Technologies** |
| **SPEAKER** | **Prof. Kaushik Roy**<br>**Purdue University, West Lafayette, IN** |
| **DATE** | **29 March 2016, Tuesday** |
| **TIME** | **12:00 pm to 1:30 pm** |
| **VENUE** | **E1-06-09 (Engineering Blk E1, Faculty of Engineering, NUS)** |

## ABSTRACT

Sub-10nm FinFET scaling presents new challenges for technology and system designers. Leakage mechanisms such as direct source to drain tunneling (DSDT) through the channel barrier, which was uncommon in longer channel bulk MOSFETs, will start dominating for sub-10nm gate lengths, necessitating careful device design using quantum mechanical simulations. We analyze the impact of DSDT in underlapped/asymmetrically doped FinFETs using 2D ballistic Physics based simulations. The increase in the effective channel length resulting from using underlap leads to significant reduction in DSDT especially in nFinFETs where the majority carriers have a lower tunneling effective mass. By including the important leakage components such as DSDT, sub-threshold leakage and direct gate oxide tunneling in the device characteristics, we derive a compact model suitable for cell library characterization and synthesize a LEON3 microprocessor and a memory subsystem. Our system level simulation results suggest that overall power consumption in sub-10nm technologies will be dominated by DSDT. We also estimate the improvements possible by using fin thickness control as a means to overcome the on-current degradation arising from gate-underlap. Finally I will discuss device and circuit design issues related to steep slope tunnel FETs.

## BIOGRAPHY

Kaushik Roy received B.Tech. degree in electronics and electrical communications engineering from the Indian Institute of Technology, Kharagpur, India, and Ph.D. degree from the electrical and computer engineering department of the University of Illinois at Urbana-Champaign in 1990. He joined the electrical and computer engineering faculty at Purdue University, West Lafayette, IN, in 1993, where he is currently Edward G. Tiedemann Jr. Distinguished Professor. His research interests include spintronics, device-circuit co-design for nano-scale Silicon and non-Silicon technologies, low-power electronics for portable computing and wireless communications, and new computing models enabled by emerging technologies. Dr. Roy has published more than 600 papers in refereed journals and conferences, holds 15 patents, graduated 65 PhD students, and is co-author of two books on Low Power CMOS VLSI Design (John Wiley & McGraw Hill). He received several awards, and has been in the editorial board of several journals and Guest Editor of several Special Issues. Dr. Roy is a fellow of IEEE.