***SEMINAR ANNOUNCEMENT***

**DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING**
**Faculty of Engineering**
Website: http://www.ece.nus.edu.sg

***Area: Integrated Circuits and Embedded Systems***

***Host: Assoc Prof Massimo Alioto***

| | | |
|---|---|---|
| **TOPIC** | **:** | **Deployment of EMC-Compliant IC Chip Techniques in Design for Hardware Security** |
| **SPEAKER** | **:** | **Prof. Makoto Nagata,<br>Kobe University** |
| **DATE** | **:** | **21 September 2018, Friday** |
| **TIME** | **:** | **4pm to 5pm** |
| **VENUE** | **:** | **E1-06-03, Engineering Block E1, Faculty of Engineering, NUS** |

## ABSTRACT

IC chips are key enablers of densely networked smart society and need to be more compliant to security and safety. The talk will start from Electromagnetic Compatibility (EMC) techniques of IC chips on the safety side, toward EMC aware design, analysis and implementation. Then, the challenges will be discussed about the deployment of such EMC techniques in the design of IC chips for the higher level of hardware security. In detail, the talk will start with Silicon experiments on electromagnetic susceptibility (noise immunity) and electromagnetic interference (noise emission) of IC chips in automotive applications, covering on-chip/in-place noise measurement (OCM) and chip-package-system board (CPS) simulation techniques. Then, the talk will evolve for side-channel leakage analysis and resiliency by design in cryptographic IC chips.

## BIOGRAPHY

Makoto Nagata received the B.S. and M.S. degrees in physics from Gakushuin University, Tokyo, in 1991 and 1993, respectively, and the Ph.D in electronics engineering from Hiroshima University, Hiroshima, in 2001. He is currently a professor of the graduate school of science, technology and innovation, Kobe University, Kobe, Japan.

His research interests include design techniques toward high performance mixed analog, RF, and digital VLSI systems with particular emphasis on power/signal/substrate integrity and electromagnetic compatibility, testing and diagnosis, three dimensional system integration, as well as their applications for hardware security and safety.

Dr. Nagata is chairing Technology Directions subcommittee for International Solid-State Circuits Conference (2018-). He was a technical program chair (2010-2011) and a symposium chair (2012-2013) for Symposium on VLSI circuits, and has served for many other conferences. He is currently an associate editor for IEEE Transactions on VLSI Systems (2015-), and also a chair for IEEE SSCS Kansai Chapter (2017-).

http://ece.nus.edu.sg/drupal/?q=node/97