Energy-Constrained Integrated Systems

SINGAPORE
December 10-14, 2018

MONDAY

8:30-10:00 am	System-Level (Over)View, Fundamental Tradeoffs, Verticals	Massimo Alioto
10:30-12:00 pm	Co-Design Methodologies and Design Space Exploration	Eduard Alarcon
1:30-3:00 pm	System-Wide Adaptive On-Chip Power Management	Eduard Alarcon
3:30-5:00 pm	Low-Energy Wireless Communications and Transceivers I	Bogdan Staszewski

TUESDAY

8:30-12:00 pm	Low-Energy Wireless Communications and Transceivers II	Bogdan Staszewski
1:30-5:00 pm	Low-Power, Information-Preserving Analog Interfaces I	Boris Murmann

WEDNESDAY

8:00-12:00 am	Low-Power, Information-Preserving Analog Interfaces II	Boris Murmann
1:30-5 pm	Ultra-Low Power and Adaptive Digital Techniques I	Massimo Alioto

THURSDAY

8:30-10:00 am	Ultra-Low Power and Adaptive Digital Techniques II	Massimo Alioto
10:30-12:00 pm	On-Chip Data Analytics and Machine Learning I	Hoi-Jun Yoo
1:30-5:00 pm	On-Chip Data Analytics and Machine Learning II	Hoi-Jun Yoo

FRIDAY

8:30-10:00 pm	Case Studies of Energy-Constrained Systems: Wearables, Biomedical	Hoi-Jun Yoo
10:30-12:00 pm	Distributed Sensors platforms and Energy-Centric System Optimization I	Jan Rabaey
1:30-3 pm	Distributed Sensors platforms and Energy-Centric System Optimization II	Jan Rabaey
3:30-5:00 pm	Case Studies of Energy-Constrained Systems: IoT, Swarms	Jan Rabaey

RATIONALE AND SCOPE

This MEAD course focuses on the design of systems-on-chip for those applications that impose a tight energy budget, as common requirement to achieve long lifetime, miniaturization and enhanced functionality in a small form factor, among the others. A tightly constrained energy budget is a common trait in several prominent applications, such as sensor nodes for the Internet of Things, wearables, biomedical and implantable devices, which the course covers through common design principles and techniques exploiting the application specificity.

This course is structured as self-contained source of knowledge and insight for both circuit designers and system architects from industry, research institutions and academia. The course distinctively emphasizes the interaction between the circuit and the system level of abstraction, providing an understanding into how solid-state circuits need to be designed with the system in mind, and how systems need to be architected based on circuit capabilities and limitations. Design driven by the circuit-system interaction indeed allows to relax the fundamental design tradeoffs at both circuit and system level (e.g., leveraging algorithmic noise resiliency to tolerate circuit imperfections, exploiting ultra-low power always-on sensor interfaces to enable event-driven execution, or making wireless communication sporadic through more intelligent systems via ultra-low power processing techniques). Such "vertical" perspective enables synergy across levels of abstraction, and offers several opportunities to reduce the energy consumption, compared to separate circuit or system optimization.

As further dimension that is distinctive of the course, circuit/system run-time co-adaptation is a common thread to reduce the circuit design margin and down-scale the system energy consumption, when the application, the task, the activation pattern, or the dataset allow. Adaptation indeed enables the exploitation of the application and the signal specificity, driving down the consumption (e.g., leveraging sparse representations to enable signal dimensionality reduction for reduced memory and wireless datarate, or exploiting circuits with run-time scalable energy-quality degradation to meet the time-varying accuracy requirement at minimum energy).

The lectures are organized in a case-study fashion for immediate fruition, enabling the usage of design techniques and abstractions in practical cases, and bridging the gap between design principles and applications. The course covers the analysis of on-going and emerging technology trends in energy-constrained integrated systems, the fundamental design tradeoffs, and the design methodologies to manage such tradeoffs. Context-aware techniques for power management, wireless communications, sensor interfaces and processing are presented, where the signal and event pattern specificity are leveraged to reduce the energy at both circuit and system level. Energy-efficient on-chip sensor data sensemaking is also addressed from the perspective of signal processing and machine learning engines for detection/classification. Finally, several case studies are comparatively analyzed to link general design principles to silicon demonstrations, highlighting the “big ideas” that are (and will be) driving further advances in energy-constrained systems.